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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,694	04/27/2001	Isao Kobayashi	35.C13077 DI	9229

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/842,694	Applicant(s) KOBAYASHI ET AL.	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/185,717* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment E filed 4/30/3 and entered as Paper No. 13 forms the basis of this Office Action. In Amendment E Applicant substantially amended claims 1 and 8. Claims 1-3 and 7-11 remain in the application. Comments on Remarks by Applicant in support of traverse of the rejections made in Office Action of Paper No. 12 are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 4/30/3 have been fully considered but they are not persuasive. In particular, Applicant's grounds for traverse are based on newly introduced claim language (idling mode emitting one of the holes, whichever is emitted in the photoelectric conversion (read) mode" (page 8); however, new art has been found over which the newly added limitation is rendered obvious. See below under "Claim Rejections – 35 USC § 103". As shown below, the accumulation or idling mode by Umibe et al indeed permits the emission of electrons, i.e., the same charge carrier type as emitted in the photoelectric conversion mode (arguments in Remarks on page 9 are therefore moot), as required by the present claim language. Therefore, new art rejections must herewith be presented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al (Japanese Patent Application Number 09-098970) in view of Umibe et al (Japanese Patent Application 06-313392). Endo et al teach (cf. Drawing 6) a photoelectric converter (cf. title and abstract) of a laminated structure (laminated regions 602, 607, 604, 605 and 606 are laminated) comprising:

a first electrode layer 602 (G) (cf. section [0050], line 3);

an insulation layer 607 (cf. section [0053], lines 5-6) inherently blocking the passage of electrons and holes;

a photoelectric conversion semiconductor layer 604 (cf. section [0050], lines 5-9);

an injection blocking layer 605 for blocking the injection of holes only (inherently so for this n-type semiconductor layer; cf. section [0050], lines 5-9) to the semiconductor photoelectric conversion layer at a time;

a second electrode layer 606 (D) (cf. section [0050], lines 5-9); and

a switching means for operating the photoelectric converter by switching through operation modes including:

(a) a photoelectric conversion mode (cf. Drawing 6(b)) for emitting electrons produced by the photon-induced electron-hole pair creation and thus accumulating holes in accordance with an amount of incident light (cf. section [0053], lines 1-17);

(b) a refresh mode (cf. Drawing 6(a)) for emitting the other of the electrons or holes, namely the holes, from the photoelectric conversion element (cf. section [0052], lines 1-4).

Although Endo et al do not specifically teach to distinguish an idling mode for emitting electrons, hence the same of the electrons or holes as emitted by the photoelectric conversion mode, from the photoelectric conversion element, it would have been obvious to include said idling mode in view of Umibe et al, who teach the inclusion of an accumulation mode whereby the G electrode becomes open with regard to direct current, thus allowing any electrons created due to incidence of light to be accumulated as a charge on a capacitor (cf. Drawing 8 and section [0051].

Motivation, for including the teaching by Umibe et al in the invention by Endo et al, stems from the improved signal-to-noise (N/S) ratio (cf. section [0053]). *Combination* of said teaching with said invention is straightforward by including the open position for said G electrode. *Success* in the implementation of said combination can therefore be reasonably expected.

1. ***Claims 2-3 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al and Umibe et al as applied to claim 1 above, and further in view of Takeda et al (5,591,963). As detailed above, claim 1 is unpatentable over Endo et al in view of Umibe et al. Neither Endo et al not Umibe et al necessarily teach the further limitation defined by claim 2. However, it would have been obvious to include said further limitation in view of Takeda et al, who teach that recombination as required for

refresh mode is too rapid unless V_{UB} reaches a sufficiently large and positive value, upon which a photoelectric current can be detected, which is the essence of the photoelectric conversion mode (cf. column 10, lines 23-28).

It would have been obvious to include the teaching of Takeda et al because a minimum detection voltage is required for providing enough acceleration to the charge carriers created in the central intrinsic portion of the device. Combination, of the teaching by Takeda et al and the invention by Endo et al and Umibe et al, is straightforward by appropriate setting of the detection and idling voltage values.

With regard to claim 3: in the directions for operation as taught by Takeda et al operation with V_{UB} small but >0 (idling mode) is preceded in Takeda et al by operation with V_{UB}=0 (refresh mode) (cf. column 11, lines 60-65). Furthermore, irregardless of this teaching, it is generally understood by those of ordinary skills in the art that when common voltage regulators are used the transition from zero to a specific minimum positive voltage necessarily involves ramping up the voltage from zero to said minimum positive voltage, from which the further limitation as defined by claim 3 follows. Therefore, claim 3 does not distinguish over the prior art.

With regard to claim 9: the potential V_{UB} in Takeda et al, which corresponds to the potential V_{dg} as defined by Applicant, can adopt zero, positive and negative values (cf. column 9, line 58 – column 10, line 2), which is understood by those of ordinary skills in the art to be a standard option in circuitry. Therefore, the further limitation as defined by claim 9 does not distinguish over the prior art.

3. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Endo et al in view of Umibe et al as applied to claim 1, and further in view of Furukawa et al (5,591,960) and Arita (4,740,710). As detailed above, claim 1 is unpatentable over Endo et al in view of Umibe et al.

Endo et al nor Umibe et al do not specifically teach the application of the photoelectric converter such that a plurality of said photoelectric elements are arranged one-dimensionally or two-dimensionally with a switching element connected for each of the photoelectric conversion elements according to the further limitation of claim 7.

However, one- and two-dimensional arrays of photoelectric elements of this kind have long been known in the art of photoelectric converter systems, as witnessed by Furukawa et al, who teach a structure consisting of a combination of pluralities of photoelectric element array sections *for the purpose of obtaining a high level signal with low noise* (cf. column 4, lines 48-55) comprising a plurality of photoelectric conversion elements, arranged two-dimensionally (cf. column 6, lines 33-37) with a switching element connected for each of the photoelectric conversion elements (cf. column 6, lines 49-56) with all the photoelectric conversion elements being divided into a plurality of n blocs (n=3, the blocks being circuit sections 1002/1102, 2002/2102, and 4002/4102; cf. column 6, lines 49-59), a light signal of all the n x m photoelectric conversion elements (m being the number of photoelectric elements in each block; undefined in claim!) divided into n=3 blocks is output (inherent in any useful application of pluralities of photoelectric converters is their output) an intersection part of the matrix wiring, which when using the photoelectric converter essentially taught by Endo et al in view of Umibe

et al comprises a laminated structure in which at least a first electrode layer, an insulating layer, a semiconductor layer and a second electrode layer are provided in this order. Furukawa et al do not necessarily teach that each layer of the laminated structure should be formed as prescribed by the further limitation of claim 7. However, *from a cost production point of view* it makes utter sense to form each said layer in this manner, because of ease of mass production; while Arita indeed teaches a photoelectric reading apparatus wherein a plurality of switches are each connected with one end of each of the photoelectric elements (diodes) (cf. column 7, lines 25-32 and Fig. 6). The teaching by Furukawa et al can be easily combined with the invention by Endo et al and Umibe et al, because creating arrays of photoelectric converters has long been considered standard in the art of photoelectric conversion apparatus, while *motivation* to include the teaching by Furukawa et al and Arita in the invention essentially taught by Endo et al and Umibe et al is prompted by the obvious advantage of high S/N ratio as obtained through including the teaching by Furukawa et al, and, furthermore, the obvious advantage of lower manufacturing cost as obtained through including the teaching by Arita.

It thus would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation of claim 7.

4. ***Claim 8*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al (Japanese Patent Application Number 09-098970) in view of Umibe et al (Japanese Patent Application No. 06-313392) and Perez-Mendez (5,596,198), or, in the

alternative, in view of Umibe et al (loc. cit.) and Sashin (4,179,100). Endo et al teach (cf. Drawing 6) a photoelectric converter (cf. title and abstract) of a laminated structure (laminated regions 602, 607, 604, 605 and 606 are laminated) comprising:

a first electrode layer 602 (G) (cf. section [0050], line 3);

an insulation layer 607 (cf. section [0053], lines 5-6) inherently blocking the passage of electrons and holes;

a photoelectric conversion semiconductor layer 604 (cf. section [0050], lines 5-9);

an injection blocking layer 605 for blocking the injection of holes only (inherently so for this n-type semiconductor layer; cf. section [0050], lines 5-9) to the semiconductor photoelectric conversion layer at a time;

a second electrode layer 606 (D) (cf. section [0050], lines 5-9); and

a switching means for operating the photoelectric converter by switching through operation modes including:

(a) a photoelectric conversion mode (cf. Drawing 6(b)) emitting electrons in accordance with an amount of incident light (cf. section [0053], lines 1-17);

(b) a refresh mode (cf. Drawing 6(a)) for emitting holes, i.e., the other of the two types (electrons, holes) from the photoelectric conversion element (cf. section [0052], lines 1-4).

Endo et al do not specifically teach to include an idling mode for emitting electrons, i.e., the same charge carrier type as in the photoelectric conversion mode, from the photoelectric conversion element. However, it would have been obvious to include an idling mode in the invention by Endo et al in view of Umibe et al, who teach

the inclusion of an accumulation mode whereby the G electrode becomes open with regard to direct current, thus allowing any electrons created due to incidence of light to be accumulated as a charge on a capacitor (cf. Drawing 8 and section [0051]).

Motivation, for including the teaching by Umibe et al in the invention by Endo et al, stems from the improved signal-to-noise (N/S) ratio (cf. section [0053]). *Combination* of said teaching with said invention is straightforward by including the open position for said G electrode. *Success* in the implementation of said combination can therefore be reasonably expected.

Endo et al nor Umibe et al necessarily teach the photoelectric converter to comprise a signal processing means, display means, electric transmission means and radiation source as further defined by claim 8.

However, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown for instance by Perez-Mendez (cf. column 6, lines 28-36). Alternatively, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown by Sashin (4,179,100) (cf. Fig. 23 and column 15, line 64 – column 65, line 15). The examiner takes official notice that the use of electrical transmission for the transmission of data to other locations for remote processing or analysis is standard in the field. Finally, any photoelectric converter needs a radiation

source for photon input, hence this aspect is inherent in a photoelectric converter system. Finally, any photoelectric converter needs a radiation source for input, hence this aspect is inherent in a photoelectric converter system.

5. ***Claim 10*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Endo in view of Umibe et al and Perez-Mendez, or, in the alternative, in view of Umibe et al and Sashin et al as applied claim 8 above, and further in view of Takeuchi et al (JP363250634A; no images available on the PTO Data Base). As detailed above, claim 8 is unpatentable over Endo et al in view of Umibe et al and Perez-Mendez, or, in the alternative, over in view of Umibe et al and Sashin et al, none of whom, however, necessarily teach the use of phosphorus as a converter of wavelength of radiation as input into a photoelectric conversion element has long been known in the art as witnessed for instance by Japanese Patent to Takeuchi et al, who teach the conversion of X-rays to light in the visible range through the use of phosphorus prior to undergoing photoelectric conversion (cf. abstract and constitution), for the purpose of making it easier to read X-ray images through said conversion.

Motivation to include this teaching by Takeuchi et al is to reduce cost by making the system more easily operable (it is understood in the art that the radiation to be investigated for the case for which the invention by Takeuchi et al is intended, i.e., X-rays, is potentially a health risk). The teaching in this regard by Takeuchi et al can be easily *combined* with the invention of claim 8 through inclusion of a phosphorous or

phosphorescent layer, which is standard in the light detection art. *Success* in combining the inventions can therefore be *reasonably expected*.

6. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al and Umibe et al as applied above to claim 1, and further in view of Hikiji et al (JP406029510A). As detailed above, claim 1 is unpatentable over Endo et al in view of Umibe et al.

Neither Endo et al nor Umibe et al necessarily teach the further limitation as defined by claim 11. However, TFT-driven photoelectric converters have long been known in the art of semiconductor image sensors, as witnessed for example by Hikiji et al, who teach the TFT-driven photoelectric converter (image sensor) to be made on the same substrate and with the same layer construction (cf. English Abstract, "Purpose", lines 1-4 and "Constitution", lines 1-7), thus increasing the compactness of the device. *Motivation* to include the teaching by Hikiji et al stems from the synergistic inclusion of the driver in the detector. *Combinability* is evident from the description of the formation of the TFT by Hikiji et al (see Abstract, "Constitution"). *Success* in implementing the combination can therefore be reasonably expected.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
July 5, 2003